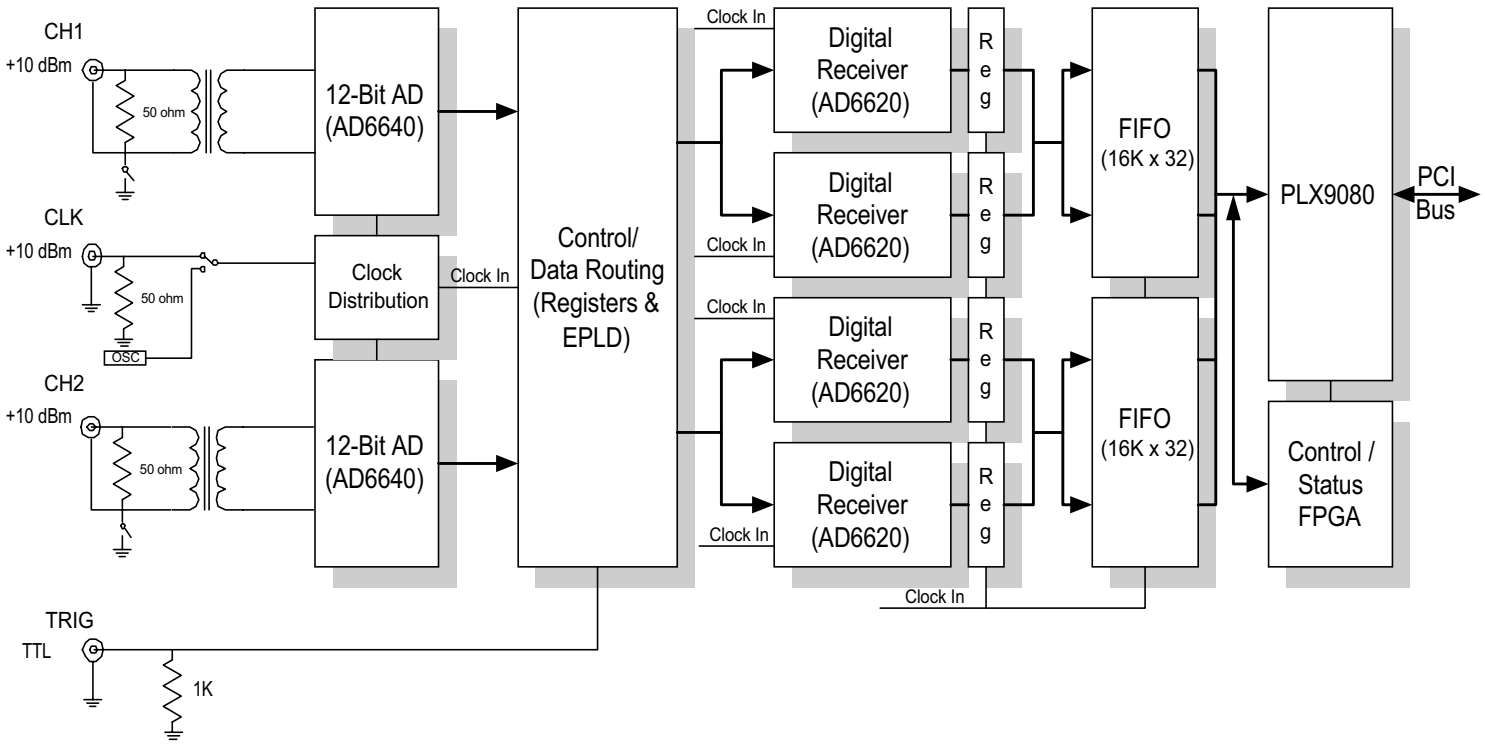
TWO CHANNEL WIDEBAND DIGITAL RECEIVER WITH INTEGRATED ANALOG INPUT - PCI BOARD ECDR-212-PCI

FEATURES

* TWO DIGITAL RECEIVER CHANNELS ON A PCI BOARD.
* ACCEPTS ANALOG INPUTS AT IF'S TO 100 MHz. USES AD6640 ANALOG/DIGITAL CONVERTERS.
* EACH RECEIVER CHANNEL CAN OPERATE WIDEBAND OR NARROWBAND (DECIMATION FROM 2 - 16K).
* DATA OUTPUT VIA PCI.
* COHERENT ON-RECEIVE CAPABILITY.
* CAN BE OPERATED IN A SINGLE CHANNEL MODE FOR VERY WIDEBAND APPLICATIONS (>5 MHz OUTPUT).
* 32 BIT SHORT LENGTH PCI BOARD.
* PCI BUS REVISION 3.1 COMPLIANT.
* EXTERNAL CLOCK INPUT OR ON-BOARD OSCILLATOR.
* FIFO DEPTH SELECTABLE FROM 8K COMPLEX SAMPLES TO 256K COMPLEX SAMPLES.
* COMPATIBLE WITH 5V OR 3.3V SIGNALING VOLTAGES.

ECDR-212-PCI BLOCK DIAGRAM



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FUNCTIONAL DESCRIPTION

This analog to digital converter and digital drop receiver board combines high speed analog to digital conversion with digital processing suitable for wideband and narrowband down conversion and filtering. Data decimation range of this product is from 2 to 16384.

Data Inputs

Data may be input to the two input channels as an analog signal. Analog signals are converted using Analog Devices AD6640, 12 bit, 65 MHz A/D converters.

A/D Clocks

The external clock is input via front panel SMA connector. Recommended signal is a sine wave +4 dBm to +10 dBm. A switch selectable on-board oscillator is also provided.

Receiver

The digital down conversion and filtering is provided by the Analog Devices AD6620 digital receiver chip. This receiver consists of four signal processing elements: A digital tuner, two fixed coefficient decimating filters, and a programmable coefficient decimating filter. The 32 bit output of each receiver (I & Q) channel is moved to a 16 K I, Q sample pair deep FIFO memory. The ECDR-412 has two such receiver channels on board.

Each of the two channels employs dual AD6620's to permit decimation in the FIR section by one-half the number of taps (coefficients). Additionally, the channel pair can be combined to provide a single channel receiver with FIR decimation by one fourth the number of taps, in support of very wideband applications.

Outputs

Data is output to the PCI bus via the PLX 9080 PCI interface chip. An on-board DMA controller is provided via the PLX 9080 PCI to Local Bus bridge to move the receiver data to the PCI bus.

Set-up and Control

All set-up and control registers are accessible via the PCI interface.

Software Support

Software device drivers and test code are available for VxWorks and Windows NT operating systems.